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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,052	10/02/2003	Jeong Hoon Choi	SI-0042	7761

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EXAMINER	
ANDREWS, LEON T	

ART UNIT	PAPER NUMBER
2416	

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10/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,052	CHOI, JEONG HOON	
	Examiner	Art Unit	
	LEON ANDREWS	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- **Claims 1, 6-7 and 9** were amended.
- **Claims 2-3 and 17-20** were cancelled.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6 and 7 are being rejected under 35 U.S.C. 103(a) as being unpatentable over Colmant et al. (Patent Number: 5,519,701) in view of Sakai (Pub. No.: US 2003/0051202 A1).

Regarding Claim 1, Colmant et al. discloses a queue assignment apparatus for a communications system (apparatus for managing storage means in a data communication system, column 1, lines 16-18), comprising:

a queue which stores data for multiple links (Fig. 1, queue manager 10 coupled to local storage 20 manages data of buses 18-1, 18-2 and 18-3, column 3, lines 16-27);

a queue assignment unit (Fig. 3A, priority control logic 27 prioritize and arbitrate a request which is outputted to a queue in the parameter RAM, column 9, lines 37-40) that assigns storage banks (Fig. 3A, BP, SIZE, THR, AFC, RP, WP) in the queue to the links (Fig. 3A, queues 1-N and links connected to the queues);

a signal detection unit (Fig. 3B, computation logic 32 for generating signals for managing storage means, column 3, lines 20-22) that detects availability of a line interface unit (Fig. 1, interfaces A, B, C); and

a data control unit (Fig. 3A, MUX 38) that reads data from the queue and writes the data in the line interface unit (via Fig. 3A, IMAC 28 to interface B (as per Fig. 1)) according to the availability of the line interface unit, wherein the queue includes at least one dual-port random access memory (DPRAM) (Fig. 7, DPRAM 51) and wherein the number of banks corresponds to a number of address bits (memory reads data stored from storage means arranged on a bit by bit basis for each frame (bank), paragraph [0038], page 2, lines 3-6) allocated in the DPRAM for one or more of the links (Fig. 7, 52 m-bit signal data, paragraph [0085], page 5, lines 5-6), and

wherein an address in the DPRAM (Fig. 7, DPRAM 61) is computed by combining a start address (Fig. 7, 54 address data from the address counter circuit 53, paragraph [0085], page 5, lines 8-10) for one of the links and bits corresponding to an extra total address (Fig. 7, 60 address data from the address counter circuit 59, paragraph [0085], page 5, lines 16-18).

Colmant et al. teaches the limitations of the claim including communication system and queue. But, Colmant et al. fails to specifically teach DPRAM, address bits and address in the DPRAM.

However, Sakai teaches (Fig. 7, DPRAM 51) and wherein the number of banks corresponds to a number of address bits (memory reads data stored from storage means arranged on a bit by bit basis for each frame (bank), paragraph [0038], page 2, lines 3-6) allocated in the DPRAM for one or more of the links (Fig. 7, 52 m-bit signal data, paragraph [0085], page 5, lines 5-6), and wherein an address in the DPRAM (Fig. 7, DPRAM 61) is computed by combining a start address (Fig. 7, 54 address data from the address counter circuit 53, paragraph [0085], page 5, lines 8-10) for one of the links and bits corresponding to an extra total address (Fig. 7, 60 address data from the address counter circuit 59, paragraph [0085], page 5, lines 16-18)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Sakai's DPRAM, address bits and address in the DPRAM because

this would have allowed the a part of communication device of a base station in the CDMA system, paragraph [0085], page 5, lines 1-3.

Regarding Claim 4, Colmant et al. discloses the apparatus of claim 1, wherein said queue assignment unit compares the number of links and the number of banks (Fig. 3B, computation logic 32 compares the value at the top of the queue with the incremented memory address, controls gating the pointer array, calculates the data amount filled in the queue and producing control signals, column 3, lines 32-44) and assigns at least one bank to each link.

Regarding Claim 5, Colmant et al. discloses the apparatus of claim 1, wherein said signal detection unit generates at least one of an empty signal and a full signal for a bank in the queue (Figs. 5A, 5B, computation logic 32 control signal is used when the queue is empty or the queue has been filled to the threshold value to update the status bits for the queue being service, column 11, lines 22-30, and circuit 88 generates a 'FULL' signal for the queue, column 11, line 44; when queue is empty, the signal, 'Qempty' will appear on bus 100, column 12, lines 43-44) corresponding to each link, and reports the state of the bank to the queue assignment unit (Fig. 3A, priority control logic 27) and the data control unit Fig. 3A, MUX 38), the data control unit reading data from and writing data to the bank (Fig. 3A, MUX 38, RP, WP) based on generation of the empty signal or full signal.

Regarding Claim 6, Colmant et al. discloses a queue assignment apparatus (Fig. 3A, priority control logic 27 prioritize and arbitrate a request which is outputted to a queue in the parameter RAM, column 9, lines 37-40) in a mobile communication system (data communication system as it relates to packet and real-time traffic such as multimedia and voice/video which is indicative of a wide range of signals, column 1, lines 15-24), comprising:

a circuit to write (Fig. 3A, parameter RAM provides a write pointer set to the base pointer, column 3, lines 23-30) data for a plurality of links in a queue (Fig. 3A, links connected to queues 1-N) of an access pointer controller (Fig. 3A, read/write pointers), the queue including a plurality of banks (Fig. 3A, BP, SIZE, THR, AFC, RP and WP in queues 1-N) for storing data for the links;

a circuit to report (Fig. 3B, computation logic 32 uses status bits in the handling of data to and from the storage queues, column 3, lines 44-47) state information indicating whether data has been written into or read from each of the banks in the queue (reading and writing of a queue through a set of status bits, column 2, lines 57-58); and

a circuit to write (Fig. 2, queue manager 10 permits reading and writing of storage, column 8, lines 58-59) the data read from one of the banks into a FIFO memory within a line interface unit (Fig. 2, queue manager writes to the local storage the words received by interface 16, column 6, lines 56-59) so that the data may be transmitted to an access pointer (Fig. 3A,

read/write pointers), wherein the queue is formed from at least one dual-port random access memory (DPRAM) (Fig. 7, DPRAM 51) and wherein the number of banks corresponds to a number of address bits (memory reads data stored from storage means arranged on a bit by bit basis for each frame (bank), paragraph [0038], page 2, lines 3-6) allocated in the DPRAM for one or more of the links (Fig. 7, 52 m-bit signal data, paragraph [0085], page 5, lines 5-6).

Colmant et al. teaches the limitations of the claim including communication system and queue. But, Colmant et al. fails to specifically teach DPRAM, address bits and address in the DPRAM.

However, Sakai teaches (Fig. 7, DPRAM 51) and wherein the number of banks corresponds to a number of address bits (memory reads data stored from storage means arranged on a bit by bit basis for each frame (bank), paragraph [0038], page 2, lines 3-6) allocated in the DPRAM for one or more of the links (Fig. 7, 52 m-bit signal data, paragraph [0085], page 5, lines 5-6), and wherein an address in the DPRAM (Fig. 7, DPRAM 61) is computed by combining a start address (Fig. 7, 54 address data from the address counter circuit 53, paragraph [0085], page 5, lines 8-10) for one of the links and bits corresponding to an extra total address (Fig. 7, 60 address data from the address counter circuit 59, paragraph [0085], page 5, lines 16-18)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Sakai's DPRAM, address bits and address in the DPRAM because this would have allowed the a part of communication device of a base station in the CDMA system, paragraph [0085], page 5, lines 1-3.

Regarding Claim 7, Colmant et al. discloses a queue assignment method (method for managing storage means in a communication system, column 1, lines 17-18) in a mobile communication system (data communication system as it relates to packet and real-time traffic such as multimedia and voice/video which is indicative of a wide range of signals, column 1, lines 15-24), comprising:

assigning a plurality of banks in a queue to store data for multiple links (Fig. 3A, BP, SIZE, THR, AFC, RP and WP in queues 1-N and links connected to the queues);

if data is to be written in a specific link (Fig. 4B, bus 68), writing the data in the relevant bank based on a write address (Fig. 4B, array 46, write pointer is written with its own unique address or when the base pointer is written, column 10, lines 60-63) and a write enable signal (first set of selected input signals provided to arrays 40-46, column 10, lines 24-25);

increasing the address of the queue (Fig. 5A, incrementer 72 increments the memory address on line 34, column 11, lines 32-33) and transmitting write pointer corresponding to the

address to a signal detection unit (Fig. 5A, calculation logic 74 determines the value and controls gating the base pointer into the write pointer array 46, column 11, lines 34-37;

comparing a read pointer and the write pointer (Fig. 5B, comparator 76 compares value at the top of the queue with the incremented memory address and gating into the read/write array 44, 46, column 11, lines 34-37) and then generating an empty signal or a full signal (Fig. 5B, AND circuit 88 generates a 'Full' signal for the queue, column 11, line 44) for transmission to a data control unit (Fig. 3A, MUX 38); and

depending on availability of a line interface unit (Fig. 2, interface 16) and an empty state of the queue (traffic upon queue 0 just started and the transmit queue is empty, column 6, lines 28-29), reading data from the queue and writing it in the line interface unit (data transmitted between interface 16 and queue 0, column 6, lines 25-26), wherein the queue includes at least one dual-port random access memory (DPRAM) (DPRAM) (Fig. 7, DPRAM 51) and wherein the number of banks corresponds to a number of address bits (memory reads data stored from storage means arranged on a bit by bit basis for each frame (bank), paragraph [0038], page 2, lines 3-6) allocated in the DPRAM for one or more of the links (Fig. 7, 52 m-bit signal data, paragraph [0085], page 5, lines 5-6).

Colmant et al. teaches the limitations of the claim including communication system and queue. But, Colmant et al. fails to specifically teach DPRAM, address bits and address in the DPRAM.

However, Sakai teaches (Fig. 7, DPRAM 51) and wherein the number of banks corresponds to a number of address bits (memory reads data stored from storage means arranged on a bit by bit basis for each frame (bank), paragraph [0038], page 2, lines 3-6) allocated in the DPRAM for one or more of the links (Fig. 7, 52 m-bit signal data, paragraph [0085], page 5, lines 5-6), and wherein an address in the DPRAM (Fig. 7, DPRAM 61) is computed by combining a start address (Fig. 7, 54 address data from the address counter circuit 53, paragraph [0085], page 5, lines 8-10) for one of the links and bits corresponding to an extra total address (Fig. 7, 60 address data from the address counter circuit 59, paragraph [0085], page 5, lines 16-18)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Sakai's DPRAM, address bits and address in the DPRAM because this would have allowed the a part of communication device of a base station in the CDMA system, paragraph [0085], page 5, lines 1-3.

Regarding Claim 8, Colmant et al. discloses the method of claim 7, wherein said assigning of banks comprises:

selecting a first link (Fig. 5A, signal line 34, column 11, line 48), checking whether the link is in use, and if the link is in use, checking whether a second link (Fig. 5B, bus for queue signal 92, column 11, line 50) is in use and increasing a link count (Fig. 5A, signal line 34 is incremented by using the fast incrementing 16 logic block 72, column 11, lines 48-49) until a last link is checked (updated pointer written back to the read or write pointer parameter RAM, column 11, lines 50-52);

if the first link is not in use, assigning a desired number of banks (Fig. 5A, add base and size parameters, QRSPTR and QSIZE to produce queue limit, column 11, lines 52-53) to the first link and assigning a start address (Fig. 5A, QFADDR, selected memory address, column 11, line 12) and an end address (Fig. 5B, QATLIMIT, incremented memory address at limit, column 11, line 20) to the link; and

assigning one or more banks (Fig. 5B, updated pointer written to the read or write pointer, column 11, lines 50-51) to the second link by increasing a start address (Fig. 5B, QINCP, incremented memory address, column 11, line 20) and end address (Fig. 5B, QATLIMIT, incremented memory address at limit, column 11, line 21) of the second link (Fig. 5B, bus for queue signal 92, column 11, line 50) by referring to the end address of the first preceding link.

Regarding Claim 9, Colmant et al. discloses the method of claim 7, wherein the writing comprises:

initializing address-related parameters (threshold parameter is reset when the base pointer is loaded, column 9, lines 5-6) of each link from a first link to a last link (Fig. 3A, links connected to the queues 1-N);

if the initialization is completed through the last link, starting a read algorithm;

checking whether there exists one item of data to be written in the queue (computation logic comprising a queue manager for handling packet and multimedia data transferred between a host and network system with a base pointer for each queue which is the starting location and a threshold value indicative of data transferred out of the queue, column 3, lines 16-26; efficient queue management algorithm for dynamically allocating and transferring data to the queues with activity, column 3, lines 50-53) beginning with the first link until the last link has been checked;

if there exists data to be written, writing the data using a write address (Fig. 5A, QFADDR memory address, column 11, line 12) and write enable signal (queue signal written back to the write parameter RAM, column 11, lines 50-52) and increasing a total address (Fig. 5A, address on signal is increased by fast incrementing 16, column 11, lines 48-49) when the writing is completed;

setting a write pointer with the increased total address, transmitting the write pointer to a signal detection unit (Fig. 3B, computation logic with the write pointer set to the base pointer, increments the memory address to control the base pointer into the write pointer to generate signals to update the queue being serviced, column 3, lines 30-37) and checking whether a current address of the link is the highest address of the bank (Fig. 3B, computation logic 32 increments the memory address, calculates the limit value at the top of the queue which is compared with the incremented memory address and controlling gating the write pointer, column 3, lines 32-36) by referring to the total address; and

if the current address is the highest address, toggling write carry for the next link, assigning the lowest bits (Fig. 3B, amount filled in the queue is equal to or greater than the threshold, the full sum of the computation logic is zero detected to produce status bits used for handling data to and from the queues, column 3, lines 42-47) to the total address, or if the current address is not the highest address, checking whether there is data for the next link.

Regarding Claim 10, Colmant et al. discloses the method of claim 9, wherein said address-related parameters include a link start address (Fig. 5A, QFADDR, selected memory address, column 11, line 12), a link end address (Fig. 5B, QINCP, incremented memory address, column 11, line 20), a total address (Fig. 5B, QATLIMIT, memory address at limit, column 11, line 21), and a write carry (Fig. 5B, adders 82 and 84 generate a carry when the queue is empty or the amount in the queue is equal to or greater than the threshold value in the queue respectively, column 11, lines 39-42).

Regarding Claim 11, Colmant et al. discloses the method of claim 9, wherein when the current address of the link has not reached the highest address of the bank, if the restart condition arises (computation logic calculates the space or room (address) available in the queue where the full sum is detected to produce almost full status, column 3, lines 37-45), said flexible queue assignment method (Fig. 3A, priority control logic 27 prioritize and arbitrate a request which is outputted to a queue in the parameter RAM, column 9, lines 37-40) further comprises initializing address-related parameters of each link (read pointer and write pointers set to the base pointer initially, column 3, lines 29-30).

Regarding Claim 12, Colmant et al. discloses the method of claim 7, wherein generating the empty signal comprises:

determining a range of each link (wide range of signals indicative of the status of packet and multimedia data the storage means, column 1, lines 21-24);

from the first link to the last link, comparing the write carry and read carry (carry when the queue is empty and a carry when the amount filled in the queue is equal to or greater than the threshold value in the queue, column 3, lines 41-43) sequentially and calculating a difference between write pointer and read pointer (write pointer value address when the next word will be written into storage with its own unique address and updated after every memory write to the queue whereas, the read pointer value used to address the next word read from the storage with its own unique address and updated after every memory read from the queue, column 10 lines 54-65); and

checking existence of data based on the difference of the pointers (read and write pointers update is to increment by 1, column 10, lines 66-67 and the add 16 block adds and yields the 1's complement of the amount filled in the queue and when the queue is empty, the signal, 'Qempty' will appear on bus 100, column 12, lines 37-44, Fig. 5B) and generating the empty signal (signal, 'Qempty' will appear on bus 100 when the queue is empty, column 12, lines 43-44) accordingly.

Regarding Claim 13, Colmant et al. discloses the method of claim 12, wherein said range of each link indicates a number of banks (Fig. 3A, BP, SIZE, THR, AFC, RP and WP to links connected to the queues 1-N) assigned to each link and is determined by using a start address

(Fig. 5A, QFADDR, selected memory address, column 11, line 12) and an end address (Fig. 5B, QINCP, incremented memory address, column 11, line 20) of each link.

Regarding Claim 14, Colmant et al. discloses the method of claim 7, wherein generating the full signal comprises:

determining a range of each link (Fig. 5A, line 34; queue manager asserts a load line, column 6, line 3; wide range of signals indicative of the storage means, column 1, lines 21-23);

from the first link to the last link, comparing the write carry and read carry (carry when the queue is empty and a carry when the amount filled in the queue is equal to or greater than the threshold value in the queue, column 3, lines 41-43) sequentially and calculating a difference of pointers (write pointer value address when the next word will be written into storage with its own unique address and updated after every memory write to the queue whereas, the read pointer value used to address the next word read from the storage with its own unique address and updated after every memory read from the queue, column 10 lines 54-65) according to the comparison; and

if the write carry and the read carry are the same, generating the full signal indicating a full or not-full state (sum of space computation logic is zero detected whereby the carry generated when the queue is empty and the carry generated when the queue is equal is equal or greater than the threshold produce full and almost full control signals, column 3, lines 41-45)

depending on whether said difference of pointers is within certain user-specified range.

Regarding Claim 15, Colmant et al. discloses the method of claim 14, wherein said difference of pointers is calculated by subtracting the read pointer from the write pointer ((write pointer value used to address the next word written into storage, column 10, lines 60-61) – (read pointer value used to address the next word to be read from storage, column 10, lines 54-55)) if the write pointer and the read pointer are the same (read and write pointers incremented by 1 until they equal the calculated limit, columns 10 and 11, lines 67 and 1 respectively), or if the write pointer and the read pointer are not the same by calculating the difference of the write pointer and the read pointer reflecting the range of link.

Regarding Claim 16, Colmant et al. discloses the method of claim 7, wherein said reading of data from the queue comprises:

checking whether the empty signal is in the not-empty state (Fig. 5B, logic block 82 or 16CO add the buses with the carry in to bit 0, so signal 'Qempty' will appear on bus 100 when the queue is empty, column 12, lines 39-44) from the first link to the last link (Fig. 5A, line 34, Fig. 5B, bus 92, line 96 and bus 98);

if a link is detected to be in the not-empty state (Fig. 5B, logic block 84), reading data through read address (Fig. 5A, QFADDR, selected memory address, column 11, line 12) and read enable signal (Fig. 5B, signal, QPCRDIF, column 12, lines 40-41) connected to the queue;

increasing read address (Fig. 5A, incrementer 72 increments the memory address on line 34, column 11, lines 32-33) and total address (Fig. 5A, address on signal is increased by fast incrementing 16, column 11, lines 48-49) by the number of data items that have been read (inputs are the signals used to update the bits for the queue being serviced, column 11, lines 27-30) and checking whether the current address of the link is equal to the highest address of the bank (Fig. 3B, computation logic 32 increments the memory address, calculates the limit value at the top of the queue which is compared with the incremented memory address, column 3, lines 32-36); and if the current address of the link is equal to the highest address, toggling read carry and initializing total address with the lowest address of the bank, thereby moving to a next link (Fig. 3B, the full sum of the computation logic is zero detected to produce status control signals where the status bits are used for handling data to and from the queues, column 3, lines 44-47).

Citation of Pertinent Prior Art

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Petersen et al. (Patent No.: US 6,504,845 B1) discloses centralized queuing for ATM node.

Sun et al. (Pub. No.: US 2003/0219026 A1) discloses method and multi-queue packet scheduling system for managing network packet traffic with minimum performance guarantees and maximum service rate control.

Sharper (Patent No.: US 6,292,491 B1) discloses distributed FIFO queuing for ATM systems.

Schramm et al. (Patent No.: US 7,016,302 B1) discloses apparatus and method for controlling queuing of data at a node on a network.

Brinkmeyer (Pub. No.: US 2001/0037354 A1) discloses computer system using a queuing system and method for managing a queue and heterogeneous data structures.

Hsu et al. (Pub. No.: US 2003/0147410 A1) discloses Ethernet switching architecture and dynamic memory allocation method for the same.

Response to Arguments

3. Applicant's arguments filed June 23, 2008 have been considered. But, in view of new grounds of rejection, the arguments are moot.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON ANDREWS whose telephone number is (571)270-1801. The examiner can normally be reached on Monday through Friday 7:30 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rao S. Seema can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LA/la
October 15, 2008

/Brenda Pham/

Primary Examiner, Art Unit 2416